A method of manufacturing a semiconductor device and a semiconductor device

TECHNICAL FIELD

The present invention relates to a method of manufacturing a semiconductor device and a semiconductor device technology, and particularly to a technology effective if applied to a method of designing a semiconductor device.

Background of the Invention

A technology for designing a semiconductor device, which has been discussed by the present inventors, is related to a technology for designing a semiconductor device having at least one substrate bias circuit under design data. There may be cases in which while a circuit cell kept low in threshold voltage exists in circuit cells of a semiconductor device to improve the operating speed, for example, a problem about a leak current arises by such a reduction in threshold voltage, thereby leading to an increase in power consumption and a thermal runaway at testing. The substrate bias circuit is such a circuit that when it is desired to suppress the leak current in the circuit cell, a predetermined voltage is applied to a well in which the circuit cell is placed, thereby to increase the threshold voltage of the circuit cell so as to suppress the leak current, whereas when the circuit cell is operated at high speed, the supply of the voltage

to the well is stopped and the threshold voltage is lowered again, thereby realizing a high-speed operation. Let's introduce a specific example of a substrate bias circuit of a semiconductor device having a CMOS circuit. As this example, there is known one wherein a first well in which one transistor constituting the CMOS circuit is disposed, and a first power supply on the high potential side are connected to each other via a first switch transistor, whereas a second well in which the other transistor constituting the CMOS circuit is disposed, and a second power supply on the reference potential side are connected to each other via a second switch transistor. Upon testing of the semiconductor device under such a configuration, the first and second switch transistors are turned off and the potential suitable for its testing is supplied from outside to thereby suppress a thermal runaway caused by a leak current. On the other hand, upon the normal operation of the semiconductor device, the first and second transistors are turned off and the first and second wells are respectively connected to the first and second power supplies to thereby prevent variations in operating speed and a latch-up or the like (see the following Patent Document 1, for example).

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PCT/WO97/21247, pp. 15-20, Figs. 1 to 5).

Summary of the Invention

However, the present inventors have found the following problems as to the design technology for the semiconductor device.

That is, when another semiconductor device that needs not use substrate bias circuits partially or wholly, is designed while taking over a semiconductor device having substrate bias circuits under design data, there is a need to re-design a wiring layout in an extensive area of a semiconductor chip or each circuit cell that needs not use the substrate bias circuits in order to fix substrate biases. Therefore, the time required to design the semiconductor device becomes long. Since a drastic circuit modification is performed, each circuit of the semiconductor device must be re-evaluated after its design, and the time taken to evaluate it becomes long. As a result of these, the TAT (Turn Around Time) of the semiconductor device becomes long.

An object of the present invention is to provide a technology capable of fixing substrate biases without taking time.

The above, other objects and novel features of the present invention will become apparent from the description of the present Specification and the accompanying drawings.

A summary of a representative one of the inventions disclosed in the present application will be explained in brief as follows:

The present invention is provided wherein when another semiconductor device that needs not use substrate bias circuits partially or wholly, is designed while taking over design data of a semiconductor device having substrate bias circuits, some of wirings are changed in such a manner that a switch for switching whether substrate biases should be applied to circuit areas that need not use the substrate bias circuits, is made invalid, and power supply voltages are applied to circuit areas that need not use the substrate bias circuits.

Brief Description of the Drawings

Fig. 1 is a typical fragmentary plan view showing a semiconductor device discussed by the present inventors;

Fig. 2 is an explanatory view of one technique of a method of designing a semiconductor device discussed by the present inventors;

Fig. 3 is an explanatory view typically depicting a semiconductor device illustrative of one embodiment of the present invention;

Fig. 4 is an overall plan view of one example of a semiconductor chip constituting the semiconductor device showing the one embodiment of the present invention;

Fig. 5 is a fragmentary enlarged plan view of an

area F shown in Fig. 4;

Fig. 6 is an explanatory view typically showing a semiconductor chip constituting a semiconductor device discussed by the present inventors;

Fig. 7 is an explanatory view typically depicting a semiconductor chip constituting a semiconductor device illustrative of one embodiment of the present invention;

Fig. 8 is a fragmentary plan view of the semiconductor device showing the one embodiment of the present invention;

Fig. 9 is a fragmentary plan view of the semiconductor device illustrative of the one embodiment of the present invention;

Fig. 10 is a cross-sectional view taken along line Y1 - Y1 of Fig. 9;

Fig. 11 is a cross-sectional view taken along line Y2 - Y2 of Fig. 9;

Fig. 12 is a cross-sectional view taken along line Y3 - Y3 of Fig. 9;

Fig. 13 is a fragmentary plan view of the semiconductor device showing the one embodiment of the present invention;

Fig. 14 is an explanatory view typically showing a semiconductor device having an SRAM module showing another embodiment of the present invention;

Fig. 15 is a circuit diagram depicting one example of a circuit configuration of a memory cell of the SRAM

module shown in Fig. 14;

Fig. 16 is an explanatory view typically showing an essential part of a semiconductor device illustrative of a further embodiment of the present invention;

Fig. 17 is an explanatory view illustrating indexes used upon determining whether a substrate bias power supply is made valid or invalid;

Fig. 18 is an explanatory view typically showing a semiconductor device illustrative of a still further embodiment of the present invention;

Fig. 19 is a fragmentary plan view of a semiconductor substrate for describing a method of designing a semiconductor device, according to a still further embodiment of the present invention;

Fig. 20 is a fragmentary plan view of the method of designing the semiconductor device, according to the still further embodiment of the present invention; and

Fig. 21 is an explanatory view typically showing a circuit configuration of a semiconductor device illustrative of a still further embodiment of the present invention.

Detailed Description of the Preferred Embodiments

Whenever circumstances require it for convenience in the following embodiments, they will be described by being divided into a plurality of sections or embodiments. However, unless otherwise specified in particular, they

are not irrelevant to one another. One thereof has to do with modifications, details and supplementary explanations of some or all of the other. When reference is made to the number of elements or the like (including the number of pieces, numerical values, quantity, range, etc.) in the following embodiments, the number thereof is not limited to a specific number and may be greater than or less than or equal to the specific number unless otherwise specified in particular and definitely limited to the specific number in principle. It is also needless to say that components (including element or factor steps, etc.) employed in the following embodiments are not always essential unless otherwise specified in particular and considered to be definitely essential in principle. Similarly, when reference is made to the shapes, positional relations and the like of the components or the like in the following embodiments, they will include ones substantially analogous or similar to their shapes or the like unless otherwise specified in particular and considered not to be definitely so in principle, etc. This is similarly applied even to the above-described numerical values and range. Preferred embodiments of the present invention will be described in detail based on the accompanying drawings. Those each having the same function in all the drawings for describing the embodiments are respectively identified by the same reference numerals and their repetitive description will

be omitted. In the present embodiments, a MIS·FET (including MOS·FET: Metal Oxide Semiconductor Field Effect Transistor as lower conception) shown as a field effect transistor is abbreviated as "MIS", a p channel type MIS·FRT is abbreviated as "pMIS" and an n channel type MIS·FET is abbreviated as "nMIS", respectively.

(Embodiment 1)

Fig. 1 typically shows a fragmentary plan view of a semiconductor device discussed by the present inventors. The present figure shows, as an example, a case in which substrate bias circuits are required.

A plurality of circuit cells BC, wirings M1a through M1i and M2a through M2f, and a slave switch circuit cell (hereinafter called switch circuit cell) SW are disposed over a main surface of a semiconductor substrate (hereinafter called substrate) 1S. Circuit cells BC are cells each of which constitutes an internal circuit of the semiconductor device. For convenience herein, a group of a plurality of the circuit cells BC arranged side by side along the horizontal direction (X direction: first direction) in Fig. 1 will be referred to as a circuit cell row. The circuit cell row is disposed over the main surface of the substrate 1S in plural stages along the vertical direction (Y direction: second direction) in Fig. 1. A basic gate circuit like, for example, an inverter circuit INV or the like is formed in each circuit cell BC. The inverter circuit INV has a pMIS

Qp and an nMIS Qn series-connected between wirings M1b and M1i. The pMIS Qp is disposed in an n well NW, and the nMIS Qn is disposed in a p well PW, respectively.

The wirings (first wirings) M1a, M1b, M1i, M2c and M2d are power supply wirings for driving the internal circuits of the semiconductor device. The wirings M1b and M2d are power supply wirings for supplying a relatively high power supply potential Vdd, and the wirings M1a, M1i and M2c are power supply wirings for supplying a relatively low power supply potential (hereinafter called reference voltage for distinction) Vss. The power supply potential Vdd is about 1.5V, for example. Also the reference potential Vss is a ground potential corresponding to 0 (zero)V, for example. The wirings M1a, M1b and M1i are formed in a first wiring layer. Here, portions extending along an X-direction wiring channel are illustrated as the wirings M1a, M1b and M1i. The wiring (M1b) for the supply of the power supply potential Vdd and the wirings (M1a and M1i) for the supply of the reference potential Vss are disposed above and below the circuit cell row so as to interpose the circuit cell row therebetween. The wirings M2c and M2d are formed in a second wiring layer. Here, portions extending along a Y-direction wiring channel are illustrated as the wirings M2c and M2d. Further, the wirings M2c and M2d are disposed in a state of intersecting (orthogonal to) the wirings M1a, M1b and M1i.

The wirings (third wirings) M2a and M2e are respectively power supply wirings for supplying substrate bias potentials Vbn and Vbp. The substrate bias potential Vbn is about 1.5V, for example. The substrate bias potential Vbp is about 3V, for example. The wirings (second wirings) M2b and M2f are respectively signal wirings for supplying control signals Vbcn and Vbcp for controlling the turning on and off of switches of the switch circuit cell. The potential of the control signal Vbcn is about 1.5V, for example, and the potential of the control signal Vbcp is about 0 (zero) V, for example. The wirings M2a, M2e, M2b and M2f are formed in a second wiring layer. Here, portions extending along the Y-direction wiring channel are illustrated as the wirings M2a, M2e, M2b and M2f. The wirings M2a, M2e, M2b and M2f are placed from side to side so as to interpose the wirings M2c and M2d therebetween. Incidentally, even though the wirings at which the power supply potential Vdd, the reference potential Vss, the substrate bias potentials Vbn and Vbp, and the control signals Vbcn and Vbcp are shown in the drawings used for the description of the embodiments (except for embodiments 3 and 4), are not connected to one another in the drawings, they are electrically connected at any points or locations in a semiconductor chip.

The switch circuit cell SW is a cell which constitutes a switch circuit for applying or unapplying

the substrate bias voltages to the n wells NW and p wells PW where the circuit cells are disposed. The switch circuit cell SW has a pMIS Qps and an nMIS Qns. The pMIS Qps has p type semiconductor regions 2P1 and 2P2 for the source and drain and a gate electrode 3G1 and is disposed in an n well NW. The p type semiconductor regions 2P1 and 2P2 are formed by introducing or implanting, for example, boron (B) into the n well NW. One semiconductor region 2P1 is electrically connected to the wiring M1c through contract holes CT1. The wiring M1c is further electrically connected to the wiring M2d via a through hole TH1. The other semiconductor region 2P2 is electrically connected to the wiring (third wiring) M1e through contact holes CT2. The wiring M1e is electrically connected to the wiring M2e via a through hole TH2. In the meanwhile, the wiring M1e is electrically connected to n^+ type semiconductor regions 4N disposed in the switch circuit cell SW and the respective circuit cells BC through a contact hole CT3 and electrically connected to the n wells NW therethrough. The gate electrode 3G1 is electrically connected to the wiring M1d. The wiring M1d is electrically connected to the wiring M2f via a through hole TH3. When such a pMIS Qps is turned off, the substrate bias potential Vbp is applied to the n wells NW, so that the threshold voltages of the pMISs Qp of the respective circuit cells BC can be rendered high, thus making it possible to suppress leak currents between the

sources and drains of the pMISs Qp. As a result, an increase in power consumption can be suppressed, and a thermal runaway caused by the leak current at testing can be suppressed. On the other hand, when the pMIS Qps is turned on, the power supply potential Vdd is applied to the n wells NW, so that the threshold voltages of the pMISs Qp of the respective circuit cells BC can be reduced, thus making it possible to increase the operating speeds of the pMISs Qp.

The nMIS Qns has n type semiconductor regions 2N1 and 2N2 for the source and drain and a gate electrode 3G2 and is disposed in a p well PW. The n type semiconductor regions 2N1 and 2N2 are formed by introducing, for example, phosphor (P) or arsenic (As) into the p well PW. One semiconductor region 2N1 is electrically connected to the wiring (third wiring) M1f through contact holes CT4. The wiring M1f is electrically connected to the wiring M2a via a through hole TH4. In the meanwhile, the wiring M1f is electrically connected to p^+ type semiconductor regions 4P respectively disposed in the switch circuit cell SW and the respective circuit cells BC through a contact hole CT5 and electrically connected to the p wells PW therethrough. The other semiconductor region 2N2 is electrically connected to the wiring M1h through contact holes CT6. The wiring M1h is electrically connected to the wiring M2c via a through contact TH5. The gate electrode 3G2 is electrically connected to the

wiring M1g. The wiring M1g is electrically connected to the wiring M2b via a through hole TH6. When such an nMIS Qns is turned off, the substrate bias potential Vbn is applied to the p wells NW, so that the threshold voltages of the nMISs Qn of the respective circuit cells BC can be rendered high, thus making it possible to suppress leak currents between the sources and drains of the nMISs Qn. As a result, an increase in power consumption can be suppressed, and a thermal runaway caused by the leak current at testing can be suppressed. On the other hand, when the nMIS Qns is turned on, the power supply potential Vss is applied to the p wells PW, so that the threshold voltages of the nMISs Qn of the respective circuit cells BC can be reduced, thus making it possible to increase the operating speeds of the nMISs Qn. Incidentally, the wirings M1c through M1h are wirings formed in the first wiring layer and formed so as to extend in the X direction.

Meanwhile, the next-generation semiconductor devices might often be designed while following some or majority of design data for a predetermined semiconductor device upon semiconductor device's design. In such a case, however, substrate bias circuits might not be needed partially or wholly. As one method in such a case, there is known, as shown in Fig. 2, a method for eliminating wirings M2a, M2b, M2e and M2f shown in areas A and B each constituting the substrate bias circuit, and a switch

circuit cell SW shown in an area C and adding wirings in areas D every circuit cells BC. In the case of this method, however, there is a need to re-design a wiring layout with the elimination of the areas A and B and perform a design change for eliminating the area C although the semiconductor device can be designed in a short period of time as compared with re-designing of all from the beginning. In addition, the wirings are added to 700 to 1200 circuit cells BC. Therefore, the time required to design the semiconductor device becomes long. Further, since such a substantial circuit modification that the wirings are added every circuit cells BC, is performed, the electrical characteristic greatly changes too. Therefore, the respective circuits of the semiconductor device must be re-evaluated after its design, and hence the time required to evaluate each circuit also becomes long. As a result of these, the TAT (Turn Around Time) of the semiconductor device becomes long.

Thus, in the present embodiment, when design data for other semiconductor device is created while following the design data for the predetermined semiconductor device, the substrate bias circuits remain unchanged, and the on/off switching operation of the switch circuit cell SW is made invalid (still kept in an on state or off state) upon operation of the semiconductor device such that the on/off switching operation thereof is not

performed. Further, part of the wiring connections is changed in such a manner that the voltages supplied to an n well NWL and a p well PWL of each circuit cell BC are fixed. Fig. 3 shows a specific example thereof. One changed with respect to Fig. 1 is only a portion equivalent to an area E. That is, the wiring M2f and the wiring M1a are electrically connected via through holes TH7 at an intersecting point thereof. Thus, since the reference potential Vss is applied to the gate electrode 3G1 of the pMIS Qps of the switch circuit cell, the pMIS Qps is always held on, so the switch operation is made invalid. Further, the wiring M2b and the wiring M1g are electrically connected via through holes TH8 at an intersecting point thereof. Thus, since the power supply potential Vdd is applied to the gate electrode 3G2 of the nMIS Qns of the switch circuit cell, the nMIS Qns is always held on so that its switch operation is made invalid. Further, the wiring M2e and the wiring M1b are electrically connected via through holes TH9 at an intersecting point thereof. Thus, since the power supply potential Vdd is applied to the wiring M1e, the n well NW of each circuit cell BC is fixed to the power supply potential Vdd. Also the wiring M2a and the wiring M1a are electrically connected via through holes TH10 at an intersecting point thereof. Thus, since the reference potential Vss is applied to the wiring M1f, the p well PW of each circuit cell BC is fixed to the reference

potential Vss. Thus, in the present embodiment, the switch operation of the switch circuit cell SW can be invalidated by only the placement of the through holes (connecting holes) TH7 through TH10 without modifying the layout of the circuits and wirings. Besides, the potentials of the n wells NW and p wells PW of a plurality of the circuit cells BC can be fixed to the power supply potential. In the case of the design technique described in Fig. 2, about two weeks are taken to change the design, whereas according to the present embodiment, only one cell library enables the design, and the time required for the design change can be almost brought to naught because there is no need to design a new cell library. Therefore, the QTAT (Quick Turn Around Time) for the design of the semiconductor device is enabled. Since there is no need to modify the wirings at each circuit cell BC, it is also unnecessary to re-evaluate the circuit of each circuit cell BC. Owing to these, the next-generation semiconductor device which follows portions that obtain high evaluations in terms of the reliability and performance of the previous-generation semiconductor device, as they are, can be manufactured in a short period of time.

A further specific one example of the semiconductor device according to the present embodiment will next be explained with reference to Figs. 4 through 13. Fig. 4 shows one example of an overall plan view of a

semiconductor chip 1C constituting the semiconductor device according to the present embodiment. Fig. 5 shows a fragmentary enlarged plan view of an area F shown in Fig. 4.

The semiconductor device according to the present embodiment is an electronic component like a general-purpose IC or ASIC (Application Specific IC) or the like employed in an electronic equipment like a cellular phone, a digital camera or a personal computer or the like. A plane square or quadrangular internal circuit area CA1 is disposed in the center of a plane square semiconductor chip 1C constituting the present semiconductor device. A plurality of macro cells MCs are disposed in the internal circuit area CA1. A plurality of circuit cell rows BCR are placed in each macro cell MC so as to be laid and packed along X and Y directions as shown in Fig. 5. In each circuit cell row BCR, a plurality of circuit cells are placed side by side along the X direction as described above. Switch circuit cells SW are disposed every circuit cell rows BCR. With connections of respective circuit cells BC in such circuit cell rows BCR, logic circuits like, for example, DSP (Digital Signal Processors) or the like, and memory circuits like, for example, RAMs (Random Access Memories), ROMs (Read Only Memories or the like are formed in the respective macro cells MC. A plurality of processors or the like in the internal circuit area CA1 perform parallel processing

while simultaneously sharing a large number of instructions and data to enhance the processing performance, thereby making it possible to process desired processing like graphic processing or the like in real time at high speed.

A peripheral circuit area CA2 is disposed between the outer periphery of the internal circuit area CA1 and the outer periphery of the semiconductor chip 1C both shown in Fig. 4. Wirings RM1 and RM2 are disposed so as to surround the outer periphery of the internal circuit area CA1. The wirings RM1 and RM2 are go-around or orbital wirings for internal circuit. Of these, the wiring RM1 has wirings M3a, M3b, M3e and M3f for substrate bias circuits. The wiring M3a is a wiring electrically connected to the wiring M2a, to which the substrate bias potential Vbn is applied. The wiring M3b is a wiring electrically connected to the wiring M2b, to which the control signal Vbcn is applied. The wiring M3e is a wiring electrically connected to the wiring M2e, to which the substrate bias potential Vbp is applied. The wiring M3f is a wiring electrically connected to the wiring M2f, to which the control signal Vbcp is applied. On the other hand, the wiring RM2 includes wirings M3c and M3d for power supplies. The wiring M3c is a wiring electrically connected to the wiring M2c, to which the power supply potential Vss is applied. The wiring M3d is a wiring electrically connected to the wiring M2d, to

which the power supply voltage Vdd is applied. The wirings M3a through M3f are formed in a third wiring layer located above the wirings M2a through M2f. In the peripheral circuit area CA2 shown in Fig. 4, a plurality of input/output circuit cells I/O are disposed around the outer peripheries of the wirings RM1 and RM2 side by side along the outer periphery of the semiconductor chip 1C. The input/output circuit cells I/O are divided into signal input/output circuit cells I/Os and power-supply input/output circuit cells I/Ov. Various interface circuits like a protection circuit for prevention of electrostatic breakdown, etc. in addition to, for example, an input circuit, an output circuit, or an input/output bidirectional circuit are formed in the signal input/output circuits I/O respectively. A substrate bias power supply circuit is disposed in an area for each input/output circuit cell I/O. Further, a plurality of pads PD are disposed around the outer peripheries of the input/output circuit cells I/O in the peripheral circuit area CA2 of Fig. 4 side by side along the outer periphery of the semiconductor chip 1C. The pads PD include signal pads and power supply pads. The pads PD are disposed every input/output circuit cells I/O referred to above. The signal pads PD are disposed for the signal input/output cells I/Os, and the power supply pads PD are disposed for the power-supply input/output circuit cells I/Ov. The pads PD may be disposed in zigzags. Thus,

since a larger number of the pads PD can be disposed in small areas, a semiconductor device that needs a number of pins can be reduced in size.

Next, Fig. 6 typically shows a semiconductor chip 1C where a substrate bias circuit is used. Symbol Vbb designates a substrate bias system potential referred to as a generic name for the substrate bias potentials Vbn and Vbp and control signals Vbcn and Vbcp. Symbol MS designates a substrate bias power supply circuit. The substrate bias power supply circuit MS is electrically connected to a switch circuit cell SW through wirings RM2 and RM1. Input/output circuit cells I/O for supplying a substrate bias control signal are electrically connected to the switch circuit cell SW through the wiring RM1. Thus, the application or non-application of the substrate bias voltages to each circuit cell BC can be controlled (see an area G shown in Fig. 6).

On the other hand, Fig. 7 typically shows a semiconductor chip 1C where a substrate bias circuit is not used as a whole. In Fig. 7 as compared with Fig. 6, a substrate bias power supply circuit MS is disconnected from wirings RM2 and RM1. The wiring RM1 is not connected to a switch circuit cell SW. The wiring RM2 for a power supply potential Vdd and a reference potential Vss is connected to the switch circuit cell SW. A substrate potential for each circuit cell BC and each input/output circuit cell I/O is fixed to the power supply potential

Vdd and the reference potential Vss (see the area G shown in Fig. 7). In this case, the substrate bias power supply circuit can be eliminated. Since large MISs, each of which belongs to a high-withstand system and is relatively thick in gate insulating film, are used as MISs constituting the substrate bias power supply circuits MS, the leak current is small. Since the substrate bias power supply circuit can be disconnected from the whole circuit in the case of the semiconductor device wherein the substrate bias circuit is not used as a whole, the power consumption of the semiconductor device can be reduced.

Next, Fig. 8 shows a specific example of the design change method of Fig. 7 where no substrate bias circuit is used. Symbol CA3 designates a go-around or orbital wiring area for internal circuit, and symbol CA4 indicates an input/output circuit area, respectively.

First of all, a design change of an area E by wiring connections in the present embodiment is identical to one mentioned above. A wiring M2a is electrically connected to a wiring M3a via a through hole TH11, a wiring M2b is electrically connected to a wiring M3b via a through hole TH12, a wiring M2c is electrically connected to a wiring M3c via a through hole TH13, a wiring M2d is electrically connected to a wiring M3d via a through hole TH14, a wiring M2e is electrically connected to a wiring M3e via a through hole TH15, and a

wiring M2f is electrically connected to a wiring M3f via a through hole TH16, respectively. Owing to such wiring connections, a substrate potential for each circuit cell row in an internal circuit area CA1, and a substrate potential for each input/output circuit cell I/O in a peripheral circuit area CA2 can be fixed to power supply potentials Vdd and Vss. According to the present embodiment, since the time taken to perform the above design change can be almost brought to naught, the QTAT for design of the semiconductor device is enabled. Since there is no need to modify the wirings at each circuit cell BC and input/output circuit cell I/O, it is also unnecessary to re-evaluate circuits for each circuit cell BC and input/output circuit cell I/O. Owing to these, the next-generation semiconductor device which follows portions that obtain high evaluations in terms of the reliability and performance of the previous-generation semiconductor device, as they are, can be manufactured in a short period of time.

Next, a design change of an area H by wiring connections in the present embodiment is identical in purpose to the wiring connections indicated by the area E and shows that a substrate bias system potential Vbb is fixed to a power supply potential Vdd and a reference potential Vss in the areas for the input/output circuit cells I/O. Wiring M3g through M3n designate go-around or orbital wirings for input/output circuits and extend and

are disposed along the outer periphery of a semiconductor chip 1C so as surround the internal circuit area CA1. In the present example, the wirings M3g through M3n are formed in, for example, a third wiring layer. The wiring M3g is essentially a wiring to which a control signal Vbcn is applied. The wiring M3h is essentially a wiring to which a substrate bias potential Vbn is applied. Further, the wiring M3i is essentially a wiring to which the control signal Vbcn is applied, and the wiring M3j is essentially a wiring to which the substrate bias potential Vbp is applied. Also the wirings M3k through M3n are respectively wirings to which the substrate potential Vss, power supply potential Vdd, reference potential Vss1 and power supply potential Vcc are applied. Of these, the outermost peripheral wirings M3n and M3m are 3.3V-system power supply wirings. The power supply potential Vcc is set to, for example, about 3.3V, and the reference potential Vss1 is set to, for example, 0 (zero)V corresponding to a ground potential. In the present embodiment herein, the wiring M3g for the control signal Vbcn is connected to a wiring M2g via a through hole TH17 and further the wiring M2g is electrically connected to the wiring M3d via through holes TH18, whereby the wiring M3g per se is fixed to the power supply potential Vdd. The wiring M3h for the substrate bias potential Vbn is connected to a wiring M2h via a through hole TH19 and further the wiring M2h is

electrically connected to the wiring M3c via through holes TH20, whereby the wiring M3h per se is fixed to the reference potential Vss. The wiring M3i for the control signal Vbcp is connected to a wiring M2i via a through hole TH21 and further the wiring M2i is electrically connected to the wiring M3c via through holes TH22, whereby the wiring M3i per se is fixed to the reference potential Vss. Further, the wiring M3i for the substrate bias potential Vbp is connected to a wiring M2j via a through hole TH23 and further the wiring M2j is electrically connected to the wiring M3d via through holes TH24, whereby the wiring M3j per se is fixed to the power supply potential Vdd. In the present embodiment as described above, the substrate potentials for all circuit cells BC and all input/output circuit cells I/O in the internal circuit area CA1 of the semiconductor chip 1C can be fixed to the power supply potential Vdd and the reference potential Vss by limiting the modification of a wiring layout to the minimum and simply changing the connections at one point of the area H. Since, even in this case, the time taken to perform the design can be shortened as compared with re-execution of all the design for the semiconductor device, the QTAT for the design of the semiconductor device is enabled. Since there is no need to modify the wirings at each circuit cell BC and input/output circuit cell I/O, it is also unnecessary to re-evaluate circuits for each circuit cell BC and

input/output circuit cell I/O. Accordingly, the next-generation semiconductor device which follows portions that obtain high evaluations in terms of the reliability and performance of the previous-generation semiconductor device, as they are, can be manufactured in a short period of time. Although, however, the change in connection at only one point of the area H has been performed here, it may be performed at several points in a dispersed form. It is thus possible to stabilize the potentials supplied to the substrate 1S. The wirings M3g through M3j for the substrate bias-system potential Vbb disposed in the peripheral circuit area CA2 may be electrically connected to the power-supply wirings M3l and M3k disposed in the peripheral circuit area CA2 to fix the substrate potentials for the circuit cells BC and input/output circuit cells I/O. Since, however, the power supply potentials to the input/output circuit cells I/O are supplied through the wirings M3l and M3k, there is a possibility that the power potentials to the input/output circuit cells I/O will change when the wirings M3g through M3j for the substrate bias-system potential Vbb are connected to the wirings M3l and M3k. It is therefore preferable that such a possibility will not be developed. The present embodiment shows where the wiring connections in both the areas E and H are done. This is because the stability of the substrate potentials for the semiconductor chip 1C can be improved by doing so.

However, it is not always necessary to perform the wiring connections in both the areas E and H. The substrate potentials can be fixed even by simply performing the wiring connections in any one of the areas. Incidentally, the wirings M2g through M2j are wirings formed in, for example, a second wiring layer and formed so to extend in the Y direction.

Next, Fig. 9 shows a specific example of the design change in the internal circuit area CA1 in Fig. 8. Even in this case, a design change of areas E1 and E2 by wiring (through-hole) connections is identical to one referred to above. Wirings M1j and M1k are wirings for supplying substrate bias potentials Vbn and Vbp to n wells NW and p wells PW of respective circuit cells BC. They are formed in a first wiring layer and formed so as to extend along the X direction. While the wiring M1j is electrically connected to a wiring M2e via a through hole TH25 at a portion where it intersects the wiring M2e, it is connected to n^+ type semiconductor regions 5N and electrically to the n wells NW through contact holes CT7. In the present embodiment, the wiring M2e is supplied with a power supply potential Vdd with the connection of the wiring M2e to a wiring M1b for the power supply potential Vdd via through holes TH9. Therefore, the n wells NW of the respective circuit cells BC can be fixed to the power supply potential Vdd through the wiring M1j electrically connected to the wiring M2e. While the

wiring M1k is electrically connected to a wiring M2a via a through hole TH26 at a portion where it intersects the wiring M2a, it is connected to p^+ type semiconductor regions 5P and electrically to the p wells PW through contact holes CT8. In the present embodiment, the wiring M2a is supplied with a reference potential Vss with the connection of the wiring M2a to a wiring M1i for the reference potential Vss via through holes TH10. Therefore, the p wells PW of the respective circuit cells BC can be fixed to the reference potential Vss through the wiring M1k electrically connected to the wiring M2a. Further, since the wirings M2a, M2b, M2e and M2f for the substrate bias-system potential Vbb can be se to the power supply potential Vdd and the reference potential Vss, the substrate potentials for input/output circuit cells I/O in the same semiconductor chip can also be fixed to the power supply potential Vdd and the reference potential Vss. Thus, since the fixing of the substrate potentials for the circuit cells BC and input/output circuit cells I/O can be carried out by only the layout or placement of the through holes TH9 and TH10 in the present embodiment, it is possible to easily perform the change of design of from the semiconductor device that needs the substrate bias circuits to the semiconductor device that needs no substrate bias circuits. Thus, the time required to design the semiconductor device can be shortened. Since there is no changes in circuit connections in the circuit

cells BC and input/output circuit cells I/O, there is no need to re-evaluate the respective circuit cells BC and input/output circuit cells I/O. Accordingly, the next-generation semiconductor device which follows portions that obtain high evaluations in terms of the reliability and performance of the previous-generation semiconductor device, as they are, can be manufactured in a short period of time.

Fig. 9 shows a case in which gate circuits like NAND circuits ND and NOR circuits NR or the like are formed in the circuit cells BC. The NAND circuit ND ad NOR circuit NR respectively have, for example, two pMISs Qp1 and Qp2, and two nMISs Qn1 and Qn2. The pMIS Qp1 has p type semiconductor regions 6P1 and 6P2 for the source and drain, and a gate electrode 3G3. The pMIS Qp2 has p type semiconductor regions 6P3 and 6P4 for the source and drain, and a gate electrode 3G4. Further, the nMIS Qn1 has n type semiconductor regions 6N1 and 6N2 for the source and drain, and the gate electrode 3G3. The nMIS Qn2 has p type semiconductor regions 6N3 and 6N4 for the source and drain, and the gate electrode 3G4. The respective circuits are respectively formed based on the layout of wirings M0 and contact holes CT9 and CT10 in the undermost layer.

One example of a vertical structure of Fig. 9 will now be explained with reference to Figs. 10 through 12. Fig. 10 is a cross-sectional view taken along line Y1 -

Y1 of Fig. 9, Fig. 11 is a cross-sectional view taken along line Y2 - Y2 of Fig. 9, and Fig. 12 is a cross-sectional view taken along line Y3 - Y3 of Fig. 9, respectively. A substrate 1S is made of, for example, p-type silicon (Si) monocrystalline. For example, trench-type separators are formed over a main surface (device forming surface) of the substrate 1S. The separators 7 are formed by embedding silicon oxide film (SiO_2 or the like) into trenches formed in the substrate 1S. As an alternative to each trench-type separator 7, the separation section may be formed by a field insulating film formed by a LOCOS (Local Oxidization of Silicon) method. The above pMISs Qps, Qp1, and Qp2 and nMISs Qns, Qn1 and Qn2 are formed in active regions defined by the separators 7. The pMISs Qps, Qp1, Qp2 and nMISs Qns, Qn1 and Qn2 respectively have gate insulating films 8 each made of, for example, the silicon oxide film or the like between the substrate 1S and the gate electrodes 3G1 through 3G4 in addition to the above configuration. Cap insulating film 9 each made of, for example, the silicon oxide film, are formed over the gate electrodes 3G1 through 3G4. Sidewalls 10 made of, for example, the silicon oxide film are formed over the sides of the gate electrodes 3G1 through 3G4 and the sides of the cap insulating films 9 placed thereover.

Wiring layers are formed over the main surface of the substrate 1S. The wiring layers are formed as a

damascene wiring structure, for example. The damascene wiring structure is a structure wherein embedded wrings are formed in wiring openings like trenches or holes or the like defined in an insulating film. The present structure is formed by, for example, depositing a conductive film over the insulating film formed with the wiring openings and thereafter removing the conductive film by polishing or the like by means of a chemical mechanical polishing (CMP) method so that the conductive film is left within the wiring openings alone. In the present embodiment, insulating films 11a through 11i, wirings M0 and M1 and plugs PL1 corresponding to some of the wiring layers are illustrated. The relatively thin insulating films 11a, 11c, 11e, 11g and 11i are respectively made of, for example, a silicon nitride film, and the relatively thick insulating films 11b, 11d, 11f and 11h are respectively made of, for example, a silicon oxide film. The wiring M0 and plug PL1 respectively have a structure wherein a thin barrier conductive film made of, for example, titanium nitride (TiN) or the like is formed over the outer periphery (sides and bottom surface) of a thick conductive film made of, for example, tungsten (W) or the like. Each wiring M1 has a structure wherein a thin barrier conductive film made of, for example, tantalum (Ta), tantalum nitride (TaN), titanium (Ti) or titanium nitride (TiN), or a laminated film or the like of films of two or more selected from these is

formed over the outer periphery (sides and bottom surface) of a thick conductive film made of, for example, copper (Cu) or the like. The layers other than the undermost or bottom layer and the top layer are constituted with copper similar to the wirings M1 of the first wiring layer as a main wiring material. The wirings M1 are respectively electrically connected to the substrate 1S via the wirings M10.

Next, Fig. 13 shows a specific example of the design change in the peripheral circuit area CA2 of Fig. 8. Symbol CA5 in Fig. 13 indicates a low threshold area in which MISs relatively low in threshold voltage are disposed, and symbol CA6 indicates a high threshold area in which MISs relatively high in threshold voltage are disposed.

Even in this case, a change of design of an area H by wiring connections is identical to one referred to above. In an area of an input/output circuit cell I/O at one location or spot, a substrate bias-system potential Vbb is connected to wirings for a power supply potential Vdd and a reference potential Vss, so that the substrate bias-system potentials Vbb for all circuit cells BC in an internal circuit area CA1 and all input/output circuit cells I/O in a peripheral circuit area CA2 can be fixed to the power supply potential Vdd and the reference potential Vss. It is thus possible to easily perform the change of design of from a semiconductor device that

needs substrate bias circuits to a semiconductor device that needs no substrate bias circuits. Thus, the time required to design the semiconductor device can be shortened. Since the wiring modification may be one spot and there is no changes in connections in the circuit cells BC and input/output circuit cells I/O per se, there is no need to re-evaluate the respective circuit cells BC and input/output circuit cells I/O. Accordingly, the next-generation semiconductor device taking over, as they are, portions that obtain high evaluations in terms of the reliability and performance of the previous-generation semiconductor device can be fabricated in a short period of time.

Each of the input/output circuit cells I/O collectively include a series of circuits necessary for the interface between an internal circuit and the outside. The interface between an external signal (e.g., 3.3V) and an internal signal (e.g., 1.5V) is performed via the input/output circuit cell I/O. Therefore, it is necessary to dispose the input/output circuit cells I/O in the vicinity of pads PD and supply at least two types of power supply voltages to the input/output circuit cells I/O. A protection circuit area ESD is an area in which a circuit for protecting the internal circuit from an excessive voltage like electrostatic breakdown or the like. In the present embodiment, protective diodes are illustrated as a protection circuit. An input buffer

circuit area IB and an output buffer circuit area OB are areas in which buffer circuits necessary for the interface between internal circuits and the outside are disposed. They operate at a power supply voltage of about 3.3V, for example. A level shifter circuit area LS1 for input is an area in which a circuit for converting a voltage level of an input signal to a voltage level at each internal circuit is disposed. The level shifter circuit area LS1 has, for example, a portion operated at a power supply voltage of about 1.5V, and a portion operated at a power supply voltage of about 3.3V. On the other hand, a level shifter circuit area LS2 for output is an area in which a circuit for converting a voltage level of a signal outputted from the internal circuit to a voltage level at the outside is disposed. The level shifter circuit area LS2 has, for example, a portion operated at a power supply voltage of about 1.5V, and a portion operated at a power supply voltage of about 3.3V. Switch circuit cells SW each having a configuration similar to the above are disposed in the level shifter circuit areas LS1 and LS2 of the respective input/output circuit cells I/O. pMISs constituting the circuits in each peripheral circuit areas CA2 are disposed in n well regions, and nMISs are disposed in p well regions. n wells and p wells in the peripheral circuit areas CA2 are circularly disposed along the outer periphery of a semiconductor chip 1C.

(Embodiment 2)

The present embodiment 2 will explain an example in which since there is a case in which substrate biases are used in pMISs and nMISs of each memory cell even in the case of a memory circuit like an SRAM (Static Random Access Memory) or the like, substrate bias circuits in such a case are invalidated.

Fig. 14 is an explanatory view typically showing a semiconductor device having an SRAM module SRM, and Fig. 15 is a circuit diagram showing one example of a circuit configuration of each memory cell SMC of the SRAM module SRM shown in Fig. 14. The SRAM module SRM will first be explained. The SRAM module SRM has a memory cell array MCA, a row decoder circuit area CD, an indirect peripheral circuit area PC, a column decoder circuit area RD, a sense amplifier circuit area SA, and an input/output circuit cell I/Om lying within the module. In the memory cell array MCA, a plurality of the memory cells SMC are disposed in the neighborhood of intersecting points of word lines WL and bit lines BL1 and BL2. For instance, a 6 MIS type memory cell SMC is illustrated in Fig. 15. That is, the memory cell SMC include drive nMISs Qnd, load pMISs Qp1, and transfer nMISs Qnt which are respectively provided two by two. Each MIS of the input/output circuit cell I/O is set lower than that of the input/output circuit cell I/O whose threshold voltage is driven at a power supply of

3.3V. In such an SRAM module SRM, substrate bias potentials Vbn and Vbp are supplied to wells for the respective MISs of the respective memory cells SMC, the row decoder circuit area CD, the indirect peripheral circuit area PC and the input/output circuit cell I/Om. Incidentally, mutually inverted signals are transmitted over the bit lines BL1 and BL2. Symbol CS indicates a chip select signal, and symbol AD indicates an address signal.

Wirings and a substrate bias circuit system will next be described. A wiring M2k is a wiring for supplying a power supply potential Vdd, and a wiring M2m is a wiring for supplying a reference potential Vss. A wiring M2n is essentially a wiring for transmitting a control signal Vbcp for each substrate bias circuit. The wiring M2n is connected to a wiring M1m via a through hole TH27 and electrically connected to a gate electrode of a pMIS Qps of a switch circuit cell SW through the wiring M1m. A wiring 2p is essentially a wiring for transmitting a control signal Vbcn for each substrate bias circuit. The wiring 2p is connected to a wiring M1n via a through hole 28 and electrically connected to a gate electrode of an nMIS Qns of the switch circuit cell SW through the wiring M1n. A wiring M2q is essentially a wiring for supplying a substrate bias potential Vbp and electrically connected to the gate of the switch circuit cell SW. A wiring M2r is essentially a wiring for supplying a substrate bias

potential Vbn and electrically connected to the drain of the nMIS Qns of the switch circuit cell SW. These wirings M2k, M2m, M2n, and M2p through M2r are formed in a second wiring layer. Also the wirings M1m and M1n are formed in a first wiring layer. Wirings M1p and M1q, which intersect (are orthogonal to) these wirings M2k, M2m, M2n and M2p through M2r, are respectively wirings essentially for supplying the substrate bias potentials Vbp and Vbn to n wells of respective pMISs of the respective memory cells SMC, the row decoder circuit area CD, the indirect peripheral circuit area PC and the input/output circuit cell I/Om and p wells of respective nMISs thereof. The wiring M1p is electrically connected to the wiring M2q via a through hole TH29, and the wiring M1q is electrically connected to the wiring M2r via a through hole TH30. Incidentally, although the wirings M1p and M1q for the memory cell array MCA are illustrated one by one to make it easy to see the drawings, a plurality of wirings M1p and M1q are actually disposed.

The above-described configuration corresponds to such a configuration that the semiconductor device which needs the substrate bias circuits originally has. A description will be made here of an example in which substrate biases become unnecessary. In this case, a design change is made by only the layout of wirings (through holes) in an area J in the present embodiment 2. That is, the wirings M2m and M1m are electrically

connected to each other via through holes TH31. Consequently, the pMIS Qps of the switch circuit cell is always held on so that its switch operation is invalidated. The wirings M2k and Mln are electrically connected to each other via through holes TH32. Thus, the nMIS Qns of the switch circuit cell is always held on so that its switch operation is invalidated. Further, the wirings M2k and Mlp are electrically connected to each other via through holes TH33. Thus, since the power supply potential Vdd is applied to the wiring Mlp, the n wells of the pMISs of the memory cell array MCA, row decoder circuit area CD, indirect peripheral circuit area PC, column decoder circuit area RD, sense amplifier circuit area SA, input/output circuit cell I/Om lying within the module are fixed to the power supply potential Vdd. The wirings M2m and Mlq are electrically connected to each other via through holes 34. Thus, since the reference potential Vss is applied to the wiring Mlq, the p wells PW of the nMISs of the memory cell array MCA, row decoder circuit area CD, indirect peripheral circuit area PC, column decoder circuit area RD, sense amplifier circuit area SA, input/output circuit cell I/Om lying within the module are fixed to the reference potential Vss.

In the present embodiment as described above, the switch operation of the switch circuit cell SW can be invalidated and the potentials of the n and p wells of

the SRAM module SRM can be fixed by only the layout of the through holes (connecting holes) TH31 through TH34 without modifying the layout of the circuits and wirings. Thus, since the time taken to perform the design change of the semiconductor device having the SRAM can be almost brought to naught, the QTAT (Quick Turn Around Time) for design thereof is enabled. Since there is no need to modify the wirings at the SRAM module SRM, it is also unnecessary to re-evaluate circuits for the SRAM module SRM. Owing to these, the next-generation semiconductor device having an SRAM module can be fabricated in a short period of time in a state of taking over points that obtain high evaluations in terms of the reliability and performance of the previous-generation semiconductor device having an SRAM module, as they are.

(Embodiment 3)

The preset embodiment 3 will explain an example in which the supply of substrate bias power supplies to only some circuit areas of a plurality of circuit areas (macro cells or modules) in a semiconductor chip is made valid, and substrate bias power supplies for other circuit areas are fixed to a power supply potential and a reference potential or the like to invalidate them.

Fig. 16 typically shows an essential part of a semiconductor device according to the present embodiment 3. For example, an input/output circuit cell I/O, an interrupt voltage controller IVC, a substrate bias

controller VBBC, a clock generator CLK, other controller UCL, a central processing unit CPU, a ROM module ROM, a first SRAM module SRM1, a digital-to-analog circuit D/A, a DMA (Direct Memory Access Controller) controller DMAC, an analog-to-digital circuit A/D, and a second SRAM module SRM2 constructing an SOC (System On Chip) are shown in the present drawing. Symbol BUS indicates an address/data bus wirings, and symbol COS indicates a control signal wiring.

Substrate biases are applied to the respective circuits in an area K, and no substrate biases are applied to the circuits in areas other than the area K. Substrate potentials are fixed to a power supply potential Vdd and a reference potential Vss in a manner similar to the embodiments 1 and 2. A method of designing a circuit group (circuit group which invalidates the substrate bias power supplies) that does not use substrate bias circuits is identical to the embodiments 1 and 2. The present embodiment shows, as an example, a case in which the substrate biases are fixed with areas L and M in the same manner as mentioned above. Namely, as to the input/output circuit cell I/O, a substrate bias-system potential Vbb for all input/output circuit cells I/O is fixed to the power supply potential Vdd and reference potential Vss at one spot in the area L. As to the circuit group for invalidating the substrate bias power supplies, the substrate bias-system potential Vbb

is fixed to the power supply potential Vdd and the reference potential Vss collectively at one spot in the area M. In any case, a substrate bias potential Vbn and a control signal Vbcp are fixed to the reference potential Vss, and a substrate bias potential Vbp and a control signal Vbcn are fixed to the power supply potential Vdd. On the other hand, as to a circuit group (circuit group for validating substrate bias power supplies) using substrate bias circuits, a substrate bias-system potential Vbb thereof is separated from the substrate bias-system potential Vbb of the circuit group for invalidating the substrate bias power supplies as indicated in an area N. That is, the substrate bias power supply systems are set so as to include two systems. Thus, even if the circuit group for validating the substrate bias power supplies and the circuit group for invalidating the same exist within the same semiconductor chip, the present embodiment is capable of flexibly coping with it. Accordingly, the present embodiment 3 is capable of obtaining an advantageous effect similar to the embodiments 1 and 2.

(Embodiment 4)

The present embodiment 4 will explain an example in which substrate bias power supplies are made valid for predetermined elements of a plurality of elements within a semiconductor chip, and substrate bias power supplies for other elements are fixed to a power supply potential

or a reference potential or the like and made invalid. A description will now be made of a case in which substrate bias power supplies for pMIS or nMIS, for example are fixed. When the threshold voltage of the pMIS or nMIS is designed high, only substrate bias power supplies of pMIS or nMIS designed low in threshold value are made valid to thereby control the threshold value of each MIS low in threshold value. It is thus possible to reduce power consumption of the semiconductor device.

Fig. 17 shows indexes used upon determining whether the substrate bias power supplies are made valid or invalid. Incidentally, Vth in the figure means threshold values. When both nMIS and pMIS are high in threshold value, the substrate bias power supplies become unnecessary. In this case, the substrate bias-system potential Vbb (substrate bias potentials Vbn and Vbp and control signals Vbcn and Vbcp) for each of the nMIS and pMIS is fixed to the power supply potential Vdd and the reference potential Vss in a manner similar to the embodiments 1 through 3. When the nMIS is high in threshold value and the pMIS is low in threshold value, the supply of the substrate bias power supplies to the pMIS is required but the supply thereof to the nMIS is not needed. Therefore, the substrate bias-system potential Vbb (substrate bias potential Vbn and control signal Vbcn) for the nMIS is fixed to the power supply potential Vdd and the reference potential Vss in a manner

similar to the embodiments 1 through 3. When the nMIS is low in threshold value and the pMIS is high in threshold value, the supply of the substrate bias power supplies to the nMIS is needed but the supply thereof to the pMIS is not needed. Therefore, the substrate bias-system potential Vbb (substrate bias potential Vbp and control signal Vbcp) for the pMIS is fixed to the power supply potential Vdd and the reference potential Vss in a manner similar to the embodiments 1 through 3. Further, when both the nMIS and pMIS are low in threshold value, the substrate bias power supplies are necessary for both the nMIS and pMIS.

Fig. 18 typically shows a specific example of the semiconductor device according to the embodiment 4. Symbol Mdd indicates a wiring for supplying a power supply potential Vdd, symbol Mss indicates a wiring for supplying a reference potential Vss, symbols Mbp1 and Mbp2 indicate wirings for supplying a substrate bias potential Vbp, symbol Mbn1 indicates a wiring for supplying a substrate bias potential Vbn, and symbol Mbn2 indicates a wiring provided to essentially supply a substrate bias potential Vbn.

In the present embodiment, all of nMISs and pMISs for a central processing unit CPU, a control circuit CC and a memory control circuit MMC of a memory module MM are respectively set as MISs low in threshold value. nMISs for a memory cell array MCA2 of the memory module

MM are set as MISs high in threshold value, and pMISs therefor are set as MISs low in threshold value. In this case, the substrate bias voltages are suitably applied to the nMISs and pMISs of the central processing unit CPU, control circuit CC and memory control circuit MMC of the memory module MM by use of a switch circuit cell SW1 of a substrate bias circuit to thereby control the operations of their nMISs and pMISs. Substrate bias voltages are suitably applied to the pMISs of the memory cell array MCA2 of the memory module MM by use of a switch circuit cell SW2 of a substrate bias circuit to thereby control the operations of the pMISs. Upon standby of the semiconductor device, for example, the substrate bias power supplies are supplied to the nMISs and pMISs of the central processing unit CPU, control circuit CC and memory control circuit MMC of the memory module MM, and the pMISs of the memory cell array MCA to increase the threshold voltages, thereby suppressing leak currents. It is thus possible to reduce power consumption of the semiconductor device. On the other hand, since there is no need to supply the substrate bias-system potential Vbb to each nMIS of the memory cell array MCA2 of the memory module MM, the wiring Mbn2 for the substrate bias potential Vbn is connected to the wiring Mss to thereby fix its potential to the reference potential Vss.

Thus, in the present embodiment 4, when the MISs low in threshold value and the MISs high in threshold

value exist in the same semiconductor chip, the substrate biases are applied to the MISs low in threshold value to control their operations, whereas the supply of the substrate bias power supplies to the MISs high in threshold value is made invalid. Thus, the leak current can be suppressed with respect to the MISs low in threshold value. In the case of the MISs high in threshold value, the substrate bias circuits (power supplies and switches) can be separated from the whole circuit of the semiconductor device. It is therefore possible to reduce the whole power consumption of the semiconductor device. In the present embodiment 4, the design for invalidation of each substrate bias circuit can be performed in a short period of time and its re-evaluation also become unnecessary in a manner similar to the embodiments 1 through 3. Even in the case of such a semiconductor device that the circuits that need the substrate bias circuit, and the circuits that need not the substrate bias circuit are provided over the same semiconductor chip, the time required to fabricate it can be shortened.

(Embodiment 5)

The present embodiment will explain a method of performing a design change by substituting each switch circuit cell with a connecting cell where substrate bias circuits are unnecessary.

Fig. 19 typically shows a fragmentary plan view of

a semiconductor device prior to invalidation of each substrate bias circuit. The switch circuit cell SW is first deleted to invalidate the substrate bias circuits. Subsequently, a connecting cell prepared in advance is taken out from a cell library and disposed in place of the switch circuit cell SW. Fig. 20 typically shows a fragmentary plan view of the semiconductor device after the connecting cell COC has been disposed. The connecting cell COC has information about through holes TH7 through TH10 which connect a wiring M2a for a substrate bias potential Vbn to a wiring M1a for a reference potential Vss, connect a wiring M2b for a control signal Vbcn to a wiring M1b for a power supply potential Vdd, connect a wiring M2e for a substrate bias potential Vbp to the wiring M1b, and connect a wiring M2f for a control signal Vbcp to the wiring M1a, respectively. Therefore, all substrate bias circuits lying in a semiconductor chip can be invalidated by only laying out the connecting cell COD at one spot of a substrate 1S. Of course, the connecting cell COC may be disposed at plural spots. When the present embodiment has circuits for invalidating the substrate bias circuits and circuits for non-invalidating the same, the connecting cell may be disposed at the switch circuit cell SW portion connected to a circuit group to be invalidated.

According to the embodiment 5, the time required to design the semiconductor device is taken as compared with

the embodiments 1 through 4. However, as compared with the case in which the semiconductor device is re-designed in all, the time required to design the semiconductor device can be shortened and re-evaluation of each circuit can be eliminated, thereby making it possible to shorten the time required to design the semiconductor device. Since the switch circuit cell constituted of relatively large MISs to perform a stable operation can be eliminated, the load can be reduced. Therefore, it is possible to reduce power consumption of the semiconductor device and improve its operating speed. Further, the area for the switch circuit cell can be used as an area for disposing each circuit cell BC by a portion corresponding to the elimination of the switch circuit cell, the number of circuit cells BC can be increased without incurring an increase in the area of a semiconductor chip. It is thus possible to promote an increase in performance of the semiconductor device.

(Embodiment 6)

The present embodiment 6 will explain an example of a method of designing a semiconductor device having a configuration wherein power supply switches are inserted between circuit modules and a power supply potential to make it possible to cut off internal power supplies in the circuit modules, thereby making it possible to realize reductions in standby currents.

Fig. 21 typically shows one example of the

semiconductor device according to the present embodiment 6. A master switch MSW, a power supply switch controller PSC, a plurality of circuit modules CM1 through CM5, a plurality of power supply switches PSW1 through PSW5 connected between the circuit modules CM1 through CM5 and a reference potential Vss, and an address/data bus wiring BUS common to the respective circuit modules CM1 through CM5 are shown in Fig. 21.

The master switch MSW is a common switch for controlling on/off operations of switch circuit cells SW connected to the circuit modules CM1 through CM5. The operation of the master switch MSW enables control for switching potentials of wells for pMISs Qp and nMISs Qn in the respective circuit modules CM1 through CM5 to substrate bias potentials Vbp and Vbn and switching the potentials thereof to the power supply potential Vdd and the reference potential Vss. Even in the present embodiment 6, those that require no substrate bias switching, can be easily re-designed by the method described in each of the embodiments 1 through 5.

Also the power supply switch controller PSC is a common switch for controlling on/off operations of the power supply switches PSW1 through PSW4. With the operation of the power supply switch controller PSC, the turning on/off of the power supply switches PSW1 through PSW4 is controlled, thereby making it possible to perform control for switching between the supply of the power

supplies to the circuit modules CM1 through CM4 and shut-off of their supply. Inserting the power supply switches PSW1 through PSW4 between the circuit modules CM1 through CM4 and the reference potential Vss respectively makes it possible to shut off the internal power supplies in the circuit modules CM1 through CM4 and realize reductions in standby currents.

Meanwhile, there might be such a demand that with the generation change of a semiconductor device or the like, for example, it is desired to always keep active some circuit modules in a semiconductor chip in the case of the next-generation semiconductor device. Where all the circuits in the semiconductor device are re-designed here, much labor and time are required in the same manner as mentioned above. In such a case, the following may be considered, for example. Now, the circuit module CM5 is illustrative of a circuit module which does not undergo power shut-off and that one wants to keep active. In the present embodiment 6, the power supply switch SW5 for supplying the power supply to the circuit module CM5 is separated from the power supply switch controller PSC. Then a gate electrode of the power supply switch SW5 is fixed to the power supply potential Vdd as indicated by an area R. Consequently, the circuit module CM5 can be always held in an active state. In the present embodiment 6 as mentioned above, a change of design of the semiconductor device can be carried out by simply

separating the power supply switch SW5 from the power supply switch controller PSC and connecting the gate electrode of the power supply switch PSW5 to the power supply potential Vdd. That is, the next-generation semiconductor device can easily be designed by using design data about the semiconductor device, having the power supply switches PSW1 through PSW5 as it is.

While the invention made above by the present inventors has been described specifically based on the illustrative embodiments, the present invention is not limited to the embodiments. It is needless to say that many changes can be made thereto within the scope not departing from the substance thereof.

For example, the wiring structure is not limited to the damascene wiring structure. The wiring structure may be configured as a normal wiring structure obtained by patterning a wiring material principally made up of, for example, aluminum.

While the above description has principally been made of the case in which the invention made by the present inventors is applied to the semiconductor device having the CMIS circuits, the semiconductor device having the SRAM modules, the semiconductor device having the SOC configuration, etc., which belong to the field of application corresponding to the background of the invention, the present invention is not limited to it. The present invention can be applied even to a

semiconductor device having a memory circuit like, for example, a DRAM (Dynamic Random Access Memory) or a flash memory (EEPROM: Electric Erasable Programmable Read Only Memory) or the like.

An advantageous effect obtained by a representative one of the inventions disclosed by the present application will be explained in brief as follows:

Some of wirings are changed in such a manner that a switch for switching whether substrate biases should be applied to circuit areas that need not use substrate bias circuits, is made invalid, and power supply voltages are applied to circuit areas that need not use the substrate bias circuits. Thus, since substrate biases can be fixed without spending time, it is possible to shorten the manufacturing time of a semiconductor device.